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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,566	08/01/2003	Philip Mattos	851963.411	2600

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EXAMINER	
WANG, TED M	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 10/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,566	MATTOS ET AL.	
	Examiner	Art Unit	
	Ted M. Wang	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,10-12,14-16,19,22-24 and 26-30* is/are rejected.

7)☒ Claim(s) *4, 5, 7-9, 13, 17, 18, 20, 21, 25 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/27/04, 3/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "32" has been used to designate both multiplexer (page 8, lines 8 and 20) and combinational logic (page 11, line 26). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

- Page 9, line 26, change "12" to --- 1, 2 ---.
- The specification is objected to because there is insufficient antecedent basis for this limitation in the claim.
    - The limitation of "wherein there are Y correlators such that in acquisition mode a correlation rate is a factor X=N (bits) x M (bit rate

factor) x Y (correlators) faster than a correlation rate in tracking mode for one of the known digital codes" as recited in claims 7 and 20 has not been taught in the specification.

- The limitation of "wherein the factor X is chosen to be substantially equal or greater than twice a number of bits in the known code, wherein all possible correlations of the code are performed before the code repeats." as recited in claims 8 and 21 has not been taught in the specification.

Appropriate correction is required.

Claim Objections

3. Claim 1 is objected to because of the following informalities:

- Claim 1, line 20, changes "that" to --- the ---.
- Claim 14, line 12, deletes --- reduced ---, since in tracking mode the sampled signal from the sampler 44 output is directly sent to the multiplexer for correlation without passing the decimator 26 that is used to generate the reduced signal.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the

differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 6, 10-12, 14-16, 19, 22-24 and 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Best (US 7,061,972) in view of Kohli (US 6,574,558).

- With regard claims 1 and 10, Best discloses a GPS receiver for processing a plurality of received broadcast signals comprising:

  a digital sampler (column 3 lines 41-44);

  a memory (Fig.2 element 44 and column 4 line 34); and

  a plurality of correlators (Fig.2 elements 50, 60A and 60B and column 6 lines 7-8), being arranged to be operable in two modes wherein:

  in an acquisition mode (column 6 lines 7-8):

  the digital sampler samples the received broadcast signals to produce a digital bit stream at a first bit rate (column 2 lines 48-51, column 5 lines 9-27 and column 5 lines 38-42, where the real time rate is, for example, 2.5 MHz, the first bit rate.);

  the memory to receive the digital bit stream and to output at a second bit rate being higher than the first bit rate (column 2 lines 48-51, column 5 lines 28-32 and column 5 lines 38-42) to the plurality of correlators (Fig.2 elements 50, 60A and 60B and column 6 lines 7-8);

the plurality of correlators (Fig.2 elements 50, 60A and 60B and column 6 lines 7-8) receive the digital bit stream at the second bit rate (column 2 lines 48-51, column 5 lines 28-32 and column 5 lines 38-42), and each of the plurality of correlators correlates the digital bit stream with a same locally generated version of one of the different known digital codes (Fig.2 elements 46, 64A and 64B, column 5 lines 61- 67 and column 6 lines 1-22); and

in a tracking mode (column 7 lines 1-5):

the digital sampler samples the received broadcast signals to produce a digital bit stream at the first bit rate (column 2 lines 48-51, column 5 lines 9-27 and column 5 lines 38-42, where the first bit rate is the real time rate, 2.5MHz) and provides that digital bit stream direct to each of the plurality of correlators (Fig.2 elements 50, 60A and 60B and column 7 lines 1-12 and 43-47), each correlator correlates the digital bit stream with a different locally generated version of one of the known digital codes (Fig.2 elements 46, 64A and 64B and column 7 lines 5-15 and column 7 lines 43-57).

Best discloses all of the subject matter as described in the above paragraph except for specifically teaching a sample reducer that reduces bits of the digital bit stream by combining groups of N bits together to produce a reduced digital bit stream.

However, Kohli teaches a sample reducer (Fig.5 element 118) that reduces bits of the digital bit stream by combining groups of N bits (column 17 lines 22-24) together to produce a reduced digital bit stream (column 17 lines 21-27, where the digital filter 118 reduces the signal from the rate of 18.67 f_0 to 2 f_0) in order to reduce the size of the memory connected to it so that the cost is reduced.

Kohli further teaches a GPS receiver that the tracking and acquisition process circuit can be implemented with a semiconductor integrated circuit (Fig.5 and column 15 lines 55-65) in order to provide fast reacquisition capabilities and reduce the number of gates required on the ASIC to reduce the cost.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to implement the digital filter 118 and memories 120, 122 as taught by Kohli into Best's acquisition circuitry to replace the signal memory 44 in order to reduce the size of the memory connected to it so that the cost is reduced and further implement the acquisition and tracking processes circuit of the Best's in an integrated circuit as taught by Kohli so as to provide fast reacquisition capabilities and reduce the number of gates required on the ASIC to reduce the cost.

- With regard claim 2, Best discloses all of the subject matter as described in the above paragraph except for specifically teaching the sample reducer comprises an adder to add the groups of N bits.

However, Kohli teaches the sample reducer comprises an adder to add the groups of N bits (column 17 lines 23-25) in order to reduce the size of the memory connected to it so that the cost is reduced.

Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to implement the digital filter 118 with an adder to add the groups of N bits and memories 120, 122 as taught by Kohli into Best's acquisition circuitry to replace the signal memory 44 in order to reduce the size of the memory connected to it so that the cost is reduced.

- With regard claim 3, Best and Kohlis' modified circuit as described in claim 2 further teaches the adder provides a digital output representative of a value of a sum of the N bits (column 17 lines 22-35, Kohli's reference) in order to reduce the filter complexity and improve the data processing speed.
- With regard claim 6, Best further discloses wherein in acquisition mode the second bit rate is a factor M higher than the first bit rate (column 5 lines 38-42).
- With regard claim 11, Best discloses all of the subject matter as described in the above paragraph except for specifically teaching wherein the memory comprises a circulating shift register.

However, Kohli further teaches wherein the memory comprises a circulating shift register (Fig.5 element 122 and column 17 lines 26-43,

where shift register element 122 has the exact same structure as that of a circulating shift register as defined in Fig.3 element 51 of the instant application.) to receive the reduced digital bit stream (Fig.5 element 119) and to output the reduced digital bit stream at the second bit rate (Fig.5 element 122 output, CAP/PUT and 108 output, DOP/OUT) to the plurality of correlators in order to provide the parallel input samples to 12 channel blocks 108 for Doppler correction (column 17 lines 36-43) so that the communication quality can be improved.

Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to implement the circulating shift register 122 along with digital (decimation) filter 118 as taught by Kohli to replace Best's memory arrangement 44 so as to improve the communication quality.

- With regard claim 12, Best and Kohlis' modified circuit as described in claim 11 further teaches wherein the circulating shift register receives the reduced digital bit stream at a rate equal to the first bit rate divided by N (column 17 lines 22-27, Kohli's reference) and circulates at the second bit rate (Fig.5 element 122 output, CAP/PUT and 108 output, DOP/OUT and column 17 lines 36-43, Kohli's reference).
- With regard claim 14, which is a method claim related to claim 1, all limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.

- With regard claim 15, which is a method claim related to claim 2, all limitation is contained in claim 2. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 16, which is a method claim related to claim 3, all limitation is contained in claim 3. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 19, which is a method claim related to claim 6, all limitation is contained in claim 6. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claims 22 and 23, which are apparatus claims related to claim 1, all limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 24, Best and Kohlis' modified circuit as described in claim 22 further teaches wherein the digital codes for the correlator (column 4 line 66, Best's reference) comprises a locally generated version of the digital code (Fig.2 elements 46 and 64A and 64B and column 6 lines 7-15 and 37-57, Best's reference) of the received broadcast signal.
- With regard claim 26, which is an apparatus claim related to claim 6, all limitation is contained in claim 6. The explanation of all the limitation is already addressed in the above paragraph.

- With regard claim 27, which is an apparatus claim related to claim 10, all limitation is contained in claim 10. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 28, which is an apparatus claim related to claim 11, all limitation is contained in claim 11. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claims 29 and 30, which are system claims related to claim 1, all limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.

Allowable Subject Matter

6. Claims 4, 5, 7-9, 13, 17, 18, 20, 21, 25 and 31 are objected to as being dependent upon an objected claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax

phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2611

Ted M. Wang